Using Hardware Performance Events for Instruction-Level Monitoring on the x86 Architecture

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Outline

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Motivation

- Why Instructions-Level Monitoring (ILM) ?

My Research

Make use of full hardware virtualization to detect malware infections and **exploitation attempts**.

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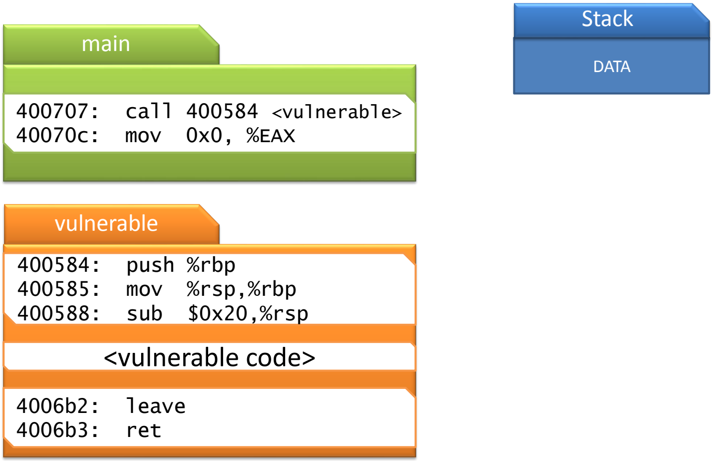

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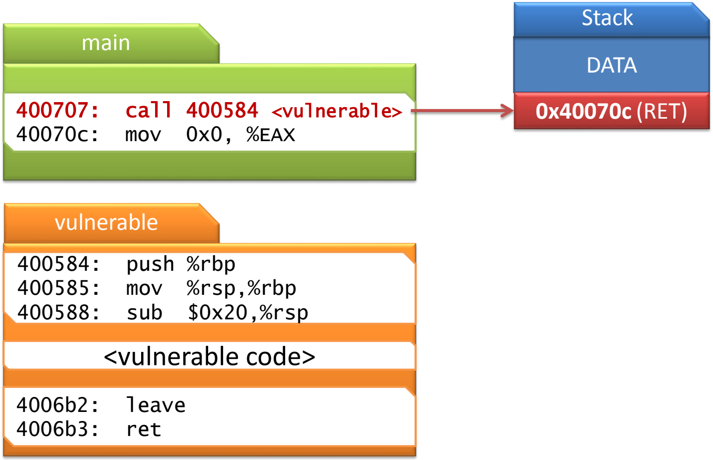

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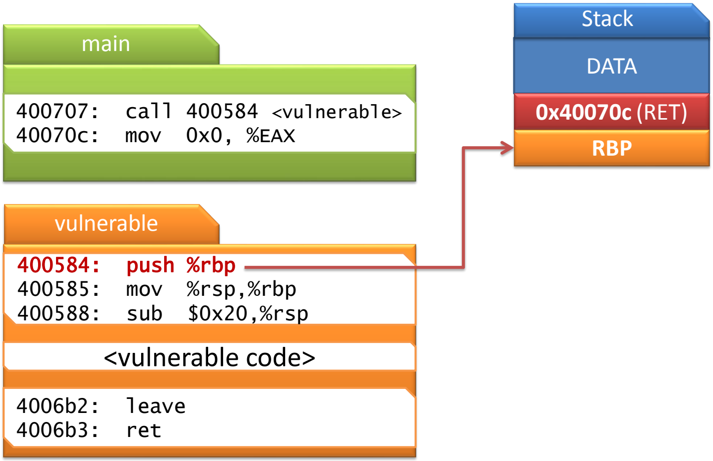

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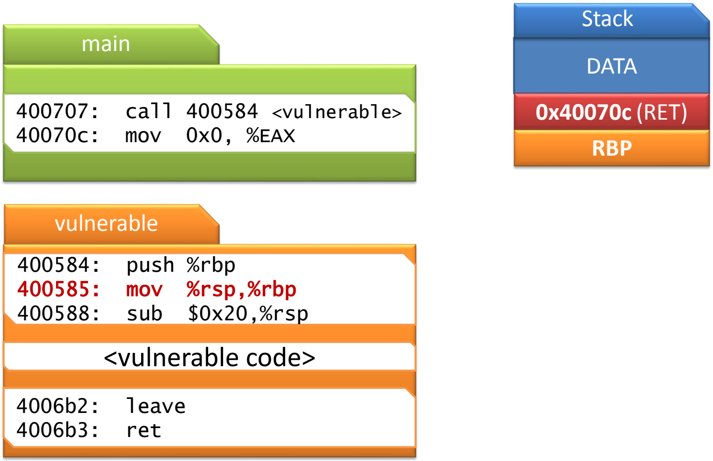

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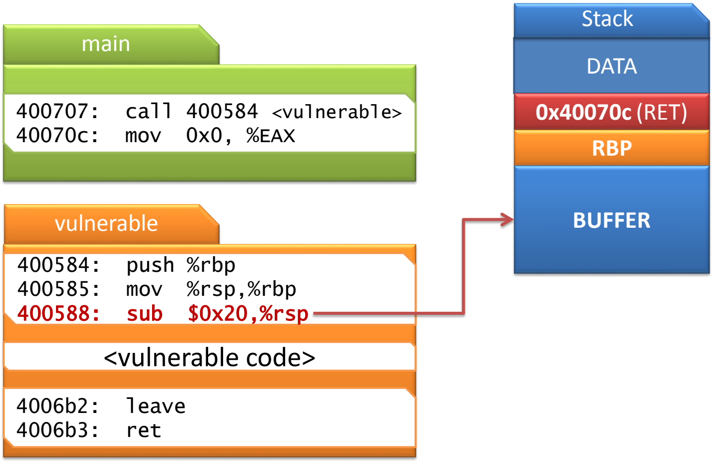

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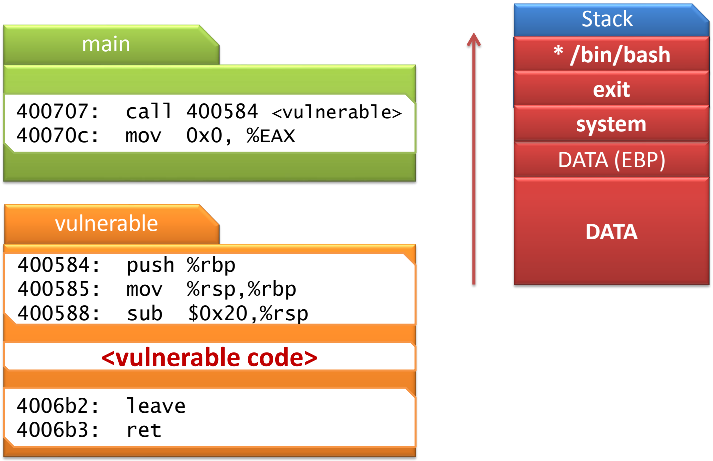

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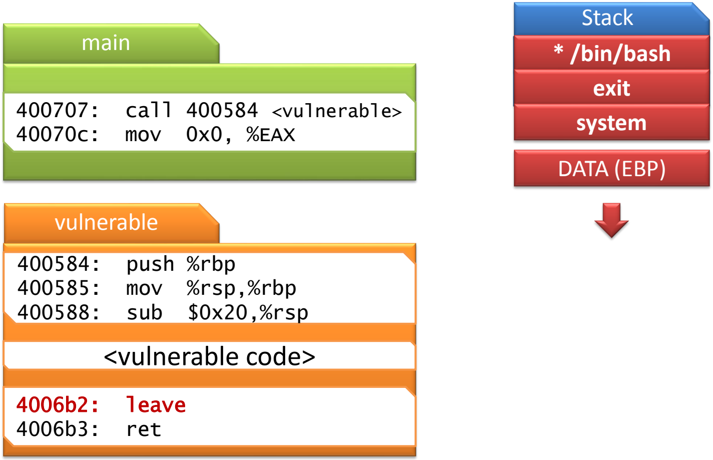

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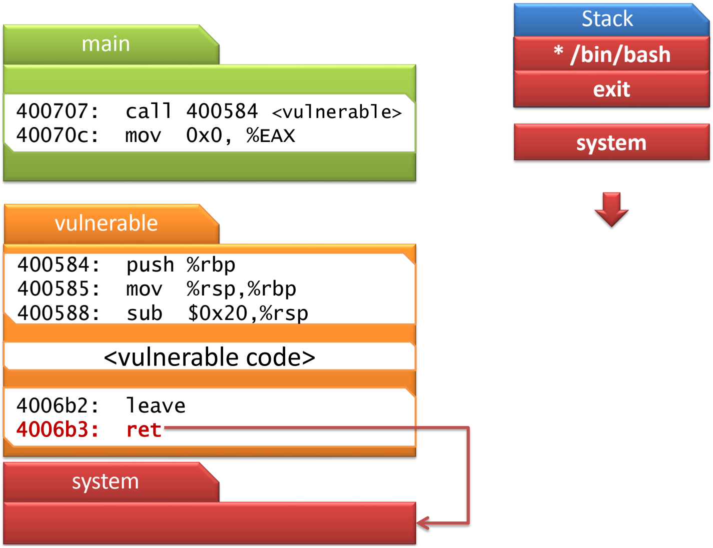

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One possible Solution

Make use of a Shadow Stack to verify the target of `return` instructions.

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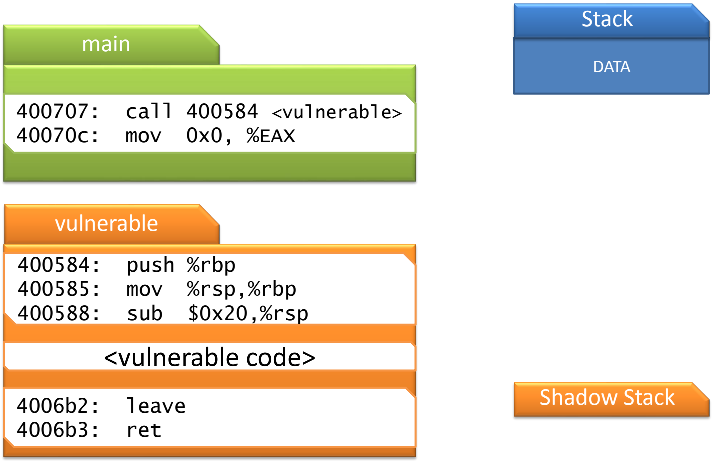

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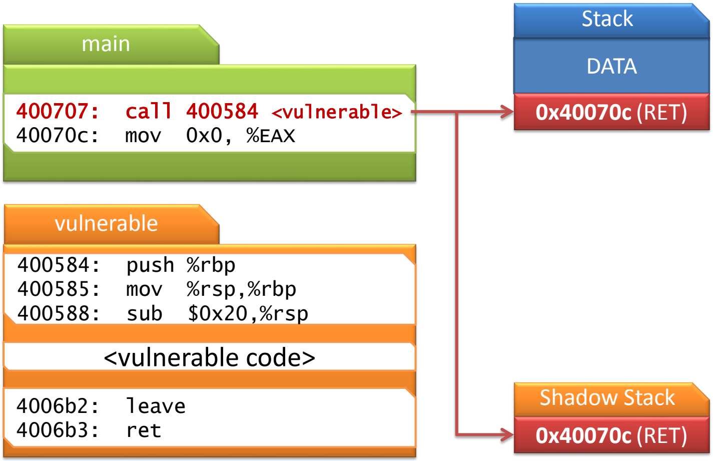

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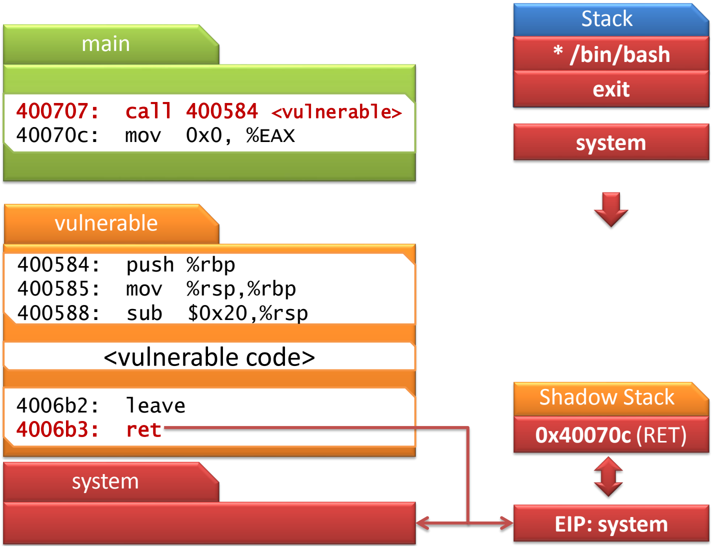

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A Shadow Stack for **return addresses** can be implemented on the **hypervisor-level** by only trapping `call` and `return` instructions.

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1. Based on full hardware virtualization
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3. Flexible

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Existing Approaches

1. **Page-Fault (PF)**-based ILM
2. **Debug Register (DR)**-based ILM
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$\Rightarrow$ None of the existing methods can provide the desired **flexbility**.

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Performance Monitoring Counters (PMCs)

▸ Overview

Performance Monitoring on the x86 architecture

- Performance Events

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Performance Monitoring on the x86 architecture

- Performance Events
- PMCs that count these events
  - Which event is counted can be programmed.
  - Can be set to raise an interrupt on overflow.

Performance Monitoring Counters (PMCs)

▸ Performance Events

- **All** instructions
- All **branch** instructions
- All **conditional branch** instructions
- All **near call** instructions
- All **near return** instructions
- All **far branch** instructions

Outline

PMC-based Instruction-level Monitoring (ILM)

▸ Trapping Performance Events

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How can we trap performance events to the hypervisor?

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1. **Interrupt Generation**: Generate an interrupt whenever the desired hardware performance event occurs.

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How can we trap performance events to the hypervisor?

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1. **Interrupt Generation**: Generate an interrupt whenever the desired hardware performance event occurs.
2. **Control Transfer**: The emitted interrupt must lead to a VM Exit.

PMC-based Instruction-level Monitoring (ILM)

▸ Trapping Performance Events: Signal Generation

Set the PMC initially to

$$\texttt{MAX\_PMC\_VALUE} - X + 1$$

where X is the number of events that should occur before the interrupt.

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$\Rightarrow$ An Interrupt will be generated.

PMC-based Instruction-level Monitoring (ILM)

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Problem: Interrupt Delivery

- There is a gap of time between the occurrence of a performance event and the interrupt delivery.
- Other performance events may go unnoticed during this period of time.
- Problem has to be solved on a case-by-case basis.

PMC-based Instruction-level Monitoring (ILM)

▸ Instruction Reconstruction (IR)

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Solution

The PMC will keep counting after an overflow occurred.

$\Rightarrow$ We know exactly how many instructions were executed before the interrupt was acknowledged.

$\Rightarrow$ Reconstruct the instruction stream and obtain the instructions that we missed.

PMC-based Instruction-level Monitoring (ILM)

▸ Instruction Reconstruction (IR)

Approach

1. Save the value of the instruction pointer on every overflow.
2. Check the value of the PMC on overflow to determine how many instructions were missed if any.
3. Disassemble every instruction starting from the last saved instruction pointer till we reach the current instruction pointer.

Example

```
40f448:  mov   %r12,%rdi            ; <====== LAST EIP
40f44b:  mov   $0x20,%esi
40f450:  mov   %rbp,%rdx
40f453:  mov   %ecx,0x28(%rsp)
40f457:  mov   %r8b,0x10(%rsp)
40f45c:  mov   %r9,0x20(%rsp)
40f461:  add   %rbp,%r12            ; <====== CURRENT EIP
```

PMC-based Instruction-level Monitoring (ILM)

What about branches?

```
40f24e:  pop    %r12                  ; <======= LAST EIP
40f250:  pop    %r13
40f252:  pop    %r14
40f254:  pop    %r15
40f256:  ret
```

Problem

The target of a branch may depend on a memory operand that may have been overwritten in the meantime.

PMC-based Instruction-level Monitoring (ILM)

LBR Stack

- Records the last taken **branches**
- Set of MSRs
    - A top-of-stack (TOS) pointer (`MSR_LASTBRANCH_TOS`)
    - A pair of MSRs for each branch that the stack can record:
      `MSR_LASTBRANCH_x_FROM_IP` ⇒ `MSR_LASTBRANCH_x_TO_LIP`
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$\Rightarrow$ Save the TOS pointer on each monitoring related interrupt.

$\Rightarrow$ All taken branches are recorded between the last saved TOS and the current TOS.

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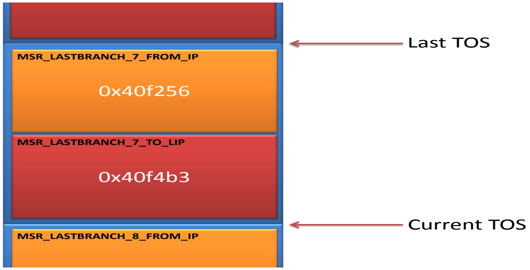

Using the LBR Stack

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40f4b3:  mov    %r12,%rdi             ; <====== CURRENT EIP
```

PMC-based Instruction-level Monitoring (ILM)

- PMCs are MSRs
- All PMC control structures are MSRs as well
- Read/Write accesses to MSRs can be intercepted from the hypervisor

$\Rightarrow$ An attacker cannot disable or manipulate the PMCs.

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- Monitored four common Linux applications at the instruction-level:

ls	(Argument: `/usr/bin`, 597 files)
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- Each application was executed multiple times using different monitoring modes:
  - PMC ALL & IR: **All** instructions & **Instruction Reconstruction**
  - TF ALL: **All** instructions
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  - PMC Shadow Stack: Only **call** & **return** instructions

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- Measured the execution time from the hypervisor for each run
- Calculated the **average slowdown factor**

Experiments & Results

▸ Results

Mode	**ls**	**tar**	**cat**	**gcc**
PMC ALL & IR	755 (18s)	1002 (3.0s)	334 (0.6s)	1263 (92s)
TF ALL	310 (7.0s)	415 (1.2s)	142 (0.3s)	545 (40s)
PMC ALL	273 (6.5s)	403 (1.2s)	126 (0.3s)	435 (32s)
PMC Branches	163 (4.0s)	259 (0.8s)	81 (0.2s)	281 (21s)
PMC Shadow Stack	95 (2.0s)	196 (0.6s)	31 (0.1s)	212 (15s)

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Security

The overall security of the mechanisms will decrease if the VM Exits are reduced.

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- PMC-based trapping
- A flexible and secure ILM mechanism
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- However, the mechanism can be significantly faster than existing hardwared-based mechanism on the x86 architecture.
- There is still a lot of room for improvements.
- More detailed experiments are needed.

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$\Rightarrow$ We encourage other researchers to explore the possibilities of **PMC-based trapping** as well as **PMC-based ILM**.

Summary

- Questions?

References I

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